ASYNC2017

San Diego, US

May 2017

23rd IEEE International Symposium on Asynchronous Circuits and Systems **CALL FOR PAPERS**

The International Symposium on Asynchronous Circuits and Systems (ASYNC) is the premier forum for researchers to present their latest findings in the area of asynchronous design. Besides a regular paper track, the conference will also hold a special industrial papers track and a fresh ideas workshop. The symposium will be hosted in San Diego, California, US, in May 2017.

REGULAR PAPERS:

Authors are invited to submit papers on any aspect of asynchronous design topics ranging from design, synthesis, and test, to asynchronous applications in system-level integration and emerging computing technologies. Topics of interest include:

- Mixed-timed circuits, GALS systems, networks-on-chips, multi-chip interconnects, and 3D integration;
- Elastic and latency-tolerant synchronous design;
- Asynchronous pipelines, architectures, CPUs, and memories;
- Asynchronous logic in ultra-low power and power-constrained systems, energy harvesting and mixed-signal/analog design;
- Asynchrony in emerging technologies, including bio, neural, nano, and quantum computing;
- CAD tools for asynchronous design, synthesis, analysis, and optimization;
- Formal methods for verification and performance/power analysis;
- Test, security, fault tolerance, and radiation-hard design;
- Asynchronous variability-tolerant, resilient design and design for manufacturing;
- Asynchronous design for neural networks and machine learning applications;
- Circuit designs, case studies, comparisons, and applications.

Submissions must report original scientific work, in 6-8 pages IEEE double-column conference format, with author information concealed. Accepted papers will be published in the IEEE digital library IEEEXplore and symposium proceedings.

INDUSTRIAL PAPERS:

ASYNC 2017 will include a special industrial workshop with papers from industry on the state-of-the-art application of asynchronous designs to both existing and emerging technologies. The topics are specifically targeted at industry and include:

- Synchronizers and clock domain crossing techniques;
- Techniques for combining asynchronous and clocked designs;
- CAD tools for integrating asynchronous circuits with clocked designs;
- Circuit designs, case studies, comparisons, and applications.

We solicit 1- to 2-page submissions, using IEEE double-column conference format. These papers will go through a separate light-weight review process. Accepted papers will be published in the IEEE digital library IEEEXplore and symposium proceedings.

FRESH IDEAS AND EMERGING HOT TOPICS WORKSHOP:

ASYNC 2017 will accommodate a special workshop to present “fresh ideas” in asynchronous design, that are not yet ready for publication as well as “emerging hot topics” to describe emerging areas of interest for asynchronous designs. We solicit 1-to-2-page submissions for the workshop, which will go through a separate light-weight review process. Accepted submissions will be handed out at the workshop.

IMPORTANT DATES:

Abstract deadline:
Nov 25, 2016

Full paper deadline:
Dec 2, 2016

Notification of acceptance:
Feb 10, 2017

Fresh ideas deadline:
Feb 24, 2017

Industrial papers deadline:
Feb 24, 2017

SYMPOSIUM COMMITTEE:

General Co-Chairs:
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*IEEE sponsorship pending

http://www.async2017.org